ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

For
ECE BRANCH

COMMON FOR
DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS
ELECTRONICS & COMMUNICATION ENGINEERING
DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING
ACADEMIC REGULATIONS R13 FOR M. Tech (REGULAR) DEGREE COURSE

Applicable for the students of M. Tech (Regular) Course from the Academic Year 2013-14 onwards

The M. Tech Degree of Jawaharlal Nehru Technological University Kakinada shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.0 AWARD OF M. Tech DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech Degree, if he pursues a course of study in not less than two and not more than four academic years.

2.2 The student shall register for all 80 credits and secure all the 80 credits.

2.3 The minimum instruction days in each semester are 90.

3.0 A. COURSES OF STUDY

The following specializations are offered at present for the M. Tech course of study.

1. M.Tech- Structural Engineering
2. M.Tech- Transportation Engineering
3. M.Tech- Infrastructure Engineering & Management
4. ME- Soil Mechanics and Foundation Engineering
5. M.Tech- Environmental Engineering
6. M.Tech-Geo-Informatics
7. M.Tech-Spatial Information Technology
8. M.Tech- Civil Engineering
11. M.Tech- Power Electronics
12. M.Tech- Power & Industrial Drives
13. M.Tech- Power Electronics & Electrical Drives
15. M.Tech- Power Electronics & Drives
16. M.Tech- Power Systems
17. M.Tech- Power Systems Engineering
18. M.Tech- High Voltage Engineering
20. M.Tech- Power System and Control
22. M.Tech- Electrical Machines and Drives
23. M.Tech- Advanced Power Systems
25. M.Tech- Control Engineering
26. M.Tech- Control Systems
27. M.Tech- Electrical Power Engineering
28. M.Tech- Power Engineering & Energy System
29. M.Tech- Thermal Engineering
30. M.Tech- CAD/CAM
32. M.Tech- Computer Aided Design and Manufacture
33. M.Tech- Advanced Manufacturing Systems
34. M.Tech-Computer Aided Analysis & Design
35. M.Tech- Mechanical Engineering Design
36. M.Tech- Systems and Signal Processing
38. M.Tech- Electronics & Communications Engineering
39. M.Tech- Communication Systems
40. M.Tech- Communication Engineering & Signal Processing
41. M.Tech- Microwave and Communication Engineering
42. M.Tech- Telematics
DECS, ECE, DECE

43. M.Tech- Digital Systems & Computer Electronics
44. M.Tech- Embedded System
45. M.Tech- VLSI
46. M.Tech- VLSI Design
47. M.Tech- VLSI System Design
48. M.Tech- Embedded System & VLSI Design
49. M.Tech- VLSI & Embedded System
50. M.Tech- VLSI Design & Embedded Systems
51. M.Tech- Image Processing
52. M.Tech- Digital Image Processing
53. M.Tech- Computers & Communication
54. M.Tech- Computers & Communication Engineering
55. M.Tech- Instrumentation & Control Systems
56. M.Tech- VLSI & Micro Electronics
57. M.Tech- Digital Electronics & Communication Engineering
58. M.Tech- Embedded System & VLSI
59. M.Tech- Computer Science & Engineering
60. M.Tech- Computer Science
61. M.Tech- Computer Science & Technology
62. M.Tech- Computer Networks
63. M.Tech- Computer Networks & Information Security
64. M.Tech- Information Technology
65. M.Tech- Software Engineering
66. M.Tech- Neural Networks
67. M.Tech- Chemical Engineering
68. M.Tech- Biotechnology
69. M.Tech- Nano Technology
70. M.Tech- Food Processing
71. M.Tech- Avionics

and any other course as approved by AICTE/ University from time to time.
### Departments offering M. Tech Programmes with specializations are noted below:

<table>
<thead>
<tr>
<th>Civil Engg.</th>
<th>1. M.Tech- Structural Engineering</th>
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<tbody>
<tr>
<td></td>
<td>2. M.Tech- Transportation Engineering</td>
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<tr>
<td></td>
<td>3. M.Tech- Infrastructure Engineering &amp; Management</td>
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<td>4. ME- Soil Mechanics and Foundation Engineering</td>
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<td>5. M.Tech- Environmental Engineering</td>
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<td>6. M.Tech-Geo-Informatics</td>
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<td>7. M.Tech-Spatial Information Technology</td>
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<td>8. M.Tech- Civil Engineering</td>
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<td>EEE</td>
<td>1. M.Tech- Power Electronics</td>
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<td>2. M.Tech- Power &amp; Industrial Drives</td>
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<td>3. M.Tech- Power Electronics &amp; Electrical Drives</td>
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<td>4. M.Tech- Power System Control &amp; Automation</td>
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<td>5. M.Tech- Power Electronics &amp; Drives</td>
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<td>11. M.Tech- Power Electronics &amp; Systems</td>
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<td>15. M.Tech- Control Engineering</td>
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<td>16. M.Tech- Control Systems</td>
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<td>17. M.Tech- Electrical Power Engineering</td>
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<td>18. M.Tech- Power Engineering &amp; Energy System</td>
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<td>ME</td>
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<td></td>
<td>2. M.Tech- CAD/CAM</td>
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<td>4. M.Tech- Computer Aided Design and Manufacture</td>
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<td>5. M.Tech- Advanced Manufacturing Systems</td>
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<tr>
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<td>6. M.Tech-Computer Aided Analysis &amp; Design</td>
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<td>7. M.Tech- Mechanical Engineering Design</td>
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<td>ECE</td>
<td>1. M.Tech- Systems and Signal Processing</td>
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<td></td>
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<td>9. M.Tech- Embedded System</td>
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<td>10. M.Tech- VLSI</td>
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<td>11. M.Tech- VLSI Design</td>
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<td>12. M.Tech- VLSI System Design</td>
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<td>14. M.Tech- VLSI &amp; Embedded System</td>
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<td>15. M.Tech- VLSI Design &amp; Embedded Systems</td>
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<td></td>
<td>20. M.Tech- Instrumentation &amp; Control Systems</td>
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<td></td>
<td>23. M.Tech- Embedded System &amp; VLSI</td>
</tr>
</tbody>
</table>

| CSE         | 1. M.Tech- Computer Science & Engineering |
|            | 2. M.Tech- Computer Science |
|            | 3. M.Tech- Computer Science & Technology |
|            | 4. M.Tech- Computer Networks |
|            | 5. M.Tech- Computer Networks & Information Security |
|            | 6. M.Tech- Information Technology |
|            | 7. M.Tech- Software Engineering |
|            | 8. M.Tech- Neural Networks |

| Others      | 1. M.Tech- Chemical Engineering |
|            | 2. M.Tech- Biotechnology |
|            | 3. M.Tech- Nano Technology |
|            | 4. M.Tech- Food Processing |
|            | 5. M.Tech- Avionics |
4.0 ATTENDANCE

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance below 65% in aggregate shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class.

4.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each mid term examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks. End semester examination is conducted for 60 marks for 5 questions to be answered out of 8 questions.
5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded based on the day-to-day performance as Internal Marks.

5.3 There shall be two seminar presentations during III semester and IV semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to reappear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate’s attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled. For re-registration the candidates have to apply to the University through the college by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required.
5.6 In case the candidate secures less than the required attendance in any re registered subject(s), he shall not be permitted to write the End Examination in that subject. He shall again re-register the subject when next offered.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher or teacher of the respective college and the second examiner shall be appointed by the university from the panel of examiners submitted by the respective college.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

6.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the Project Review Committee (PRC) shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 A candidate shall submit his status report in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after
successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

6.9 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the University.

6.10 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate’s work as one of the following:
A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination.

6.11 If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the University.
7.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

<table>
<thead>
<tr>
<th>Class Awarded</th>
<th>% of marks to be secured</th>
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</thead>
<tbody>
<tr>
<td>First Class with Distinction</td>
<td>70% and above (Without any Supplementary Appearance )</td>
</tr>
<tr>
<td>First Class</td>
<td>Below 70% but not less than 60% 70% and above (With any Supplementary Appearance )</td>
</tr>
<tr>
<td>Second Class</td>
<td>Below 60% but not less than 50%</td>
</tr>
</tbody>
</table>

The marks in internal evaluation and end examination shall be shown separately in the memorandum of marks.

8.0 WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the university or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

4.0 TRANSITORY REGULATIONS ( for R09 )

9.1 Discontinued or detained candidates are eligible for re-admission into same or equivalent subjects at a time as and when offered.

9.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per R13 academic regulations.

10. GENERAL

10.1 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

10.2 The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

10.4 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.
# MALPRACTICES RULES
## DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

<table>
<thead>
<tr>
<th>Nature of Malpractices/ Improper conduct</th>
<th>Punishment</th>
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<tbody>
<tr>
<td><strong>If the candidate:</strong></td>
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<tr>
<td>1. (a) Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only.</td>
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<tr>
<td>(b) Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the examination hall in respect of any matter.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.</td>
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<tr>
<td>2. Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project</td>
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<td>(theory or practical) in which the candidate is appearing.</td>
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<td>3.</td>
<td>Impersonates any other candidate in connection with the examination.</td>
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<td>4.</td>
<td>Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after</td>
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<td>5.</td>
<td>Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.</td>
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<td>6.</td>
<td>Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or</td>
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<td><strong>outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.</strong></td>
<td>Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.</td>
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<tr>
<td><strong>7. Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.</strong></td>
<td>Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.</td>
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</table>
|**8. Possess any lethal weapon or firearm in the examination hall.** | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining
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<tr>
<td>9.</td>
<td>If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.</td>
<td>Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.</td>
</tr>
<tr>
<td>10.</td>
<td>Comes in a drunken condition to the examination hall.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.</td>
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<tr>
<td>11.</td>
<td>Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.</td>
<td>Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.</td>
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<tr>
<td>12.</td>
<td>If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.</td>
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</table>
Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.

2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
   (i) A show cause notice shall be issued to the college.
   (ii) Impose a suitable fine on the college.
   (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.
Prohibition of ragging in educational institutions Act 26 of 1997

Salient Features

⇒ Ragging within or outside any educational institution is prohibited.
⇒ Ragging means doing an act which causes or is likely to cause Insult or Annoyance of Fear or Apprehension or Threat or Intimidation or outrage of modesty or Injury to a student

<table>
<thead>
<tr>
<th>Imprisonment upto</th>
<th>Fine Upto</th>
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<tbody>
<tr>
<td>6 Months</td>
<td>Rs. 1,000/-</td>
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<tr>
<td>1 Year</td>
<td>Rs. 2,000/-</td>
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<td>2 Years</td>
<td>Rs. 5,000/-</td>
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<td>5 Years</td>
<td>Rs. 10,000/-</td>
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<tr>
<td>10 Months</td>
<td>Rs. 50,000/-</td>
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</tbody>
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In Case of Emergency CALL TOLL FREE NO.: 1800 - 425 - 1288

LET US MAKE JNTUK A RAGGING FREE UNIVERSITY
ABSOLUTELY NO TO RAGGING

1. Ragging is prohibited as per Act 26 of A.P. Legislative Assembly, 1997.
2. Ragging entails heavy fines and/or imprisonment.
3. Ragging invokes suspension and dismissal from the College.
4. Outsiders are prohibited from entering the College and Hostel without permission.
5. Girl students must be in their hostel rooms by 7.00 p.m.
6. All the students must carry their Identity Card and show them when demanded.
7. The Principal and the Wardens may visit the Hostels and inspect the rooms any time.

In Case of Emergency CALL TOLL FREE NO. : 1800 - 425 - 1288
LET US MAKE JNTUK A RAGGING FREE UNIVERSITY
# DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Specialization: Communication Systems

## COURSE STRUCTURE

### I SEMESTER

<table>
<thead>
<tr>
<th>S.No</th>
<th>Name of the Subject</th>
<th>L</th>
<th>P</th>
<th>C</th>
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<tbody>
<tr>
<td>1</td>
<td>1. Digital System Design</td>
<td>4</td>
<td>-</td>
<td>3</td>
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<tr>
<td>2</td>
<td>2. Detection &amp; Estimation Theory</td>
<td>4</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>3. Digital Data Communications</td>
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**TOTAL 20**

### II SEMESTER

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<td>4. Wireless Communications &amp; Networks</td>
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### III – SEMESTER

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### IV – SEMESTER

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The project will be evaluated at the end of the IV Semester.
UNIT-I

Minimization Procedures and CAMP Algorithm:
Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II

PLA Design, Minimization and Folding Algorithms:
Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT-III

Design of Large Scale Digital Systems:
Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV

Fault Diagnosis in Combinational Circuits:
Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean
difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V

Fault Diagnosis in Sequential Circuits:

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXTBOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

UNIT –I

Random Processes:
Discrete Linear Models, Markov Sequences and Processes, Point Processes, and Gaussian Processes.

UNIT –II

Detection Theory:
Basic Detection Problem, Maximum A-posteriori Decision Rule, Minimum Probability of Error Classifier, Bayes Decision Rule, Multiple-Class Problem (Bayes)- minimum probability error with and without equal a priori probabilities, Neyman-Pearson Classifier, General Calculation of Probability of Error, General Gaussian Problem, Composite Hypotheses.

UNIT –III

Linear Minimum Mean-Square Error Filtering:
Linear Minimum Mean Squared Error Estimators, Nonlinear Minimum Mean Squared Error Estimators. Innovations, Digital Wiener Filters with Stored Data, Real-time Digital Wiener Filters, Kalman Filters.

UNIT –IV

Statistics:

UNIT –V

Estimating the Parameters of Random Processes from Data:
TEXT BOOKS:


REFERENCE BOOKS:


3. Introduction to Statistical Signal Processing with Applications - Srinath, Rajasekaran, Viswanathan, 2003, PHI.


UNIT-I

**Digital Modulation Schemes:**

BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Efficiency, Carrier Recovery, Clock Recovery.

UNIT-II

**Basic Concepts of Data Communications, Interfaces and Modems:**


UNIT-III

**Error Correction:** Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code

**Data Link Control:** Line Discipline, Flow Control, Error Control


UNIT-IV

**Multiplexing:** Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, DSL.

**Local Area Networks:** Ethernet, Other Ether Networks, Token Bus, Token Ring, FDDI.

**Metropolitan Area Networks:** IEEE 802.6, SMDS

**Switching:** Circuit Switching, Packet Switching, Message Switching.

**Networking and Interfacing Devices:** Repeaters, Bridges, Routers, Gateway, Other Devices.
UNIT-V

Multiple Access Techniques:

Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization, Frequency- Division Multiple Access (FDMA), Time- Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA), OFDM and OFDMA.

TEXT BOOKS:


REFERENCE BOOKS:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
<table>
<thead>
<tr>
<th>UNIT –I</th>
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<tr>
<td><em>Review of DFT, FFT, IIR Filters and FIR Filters:</em></td>
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<tr>
<td><em>Multi Rate Signal Processing:</em> Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design &amp; Implementation for sampling rate conversion.</td>
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<td><em>Applications of Multi Rate Signal Processing:</em></td>
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<td><em>Non-Parametric Methods of Power Spectral Estimation:</em> Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch &amp; Blackman-Tukey methods, Comparison of all Non-Parametric methods</td>
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<td><em>Implementation of Digital Filters:</em></td>
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<td>Introduction to filter structures (IIR &amp; FIR), Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.</td>
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power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS


REFERENCE BOOKS:

UNIT I

**Fourier Analysis:** Fourier series, Examples, Fourier Transform, Properties of Fourier Transform, Examples of Fourier transform, sampling theorem, Partial sum and Gibbs phenomenon, Fourier analysis of Discrete time Signals, Discrete Fourier Transform.

**Time – Frequency Analysis:** Window function, Short Time Fourier Transform, Discrete Short Time Fourier Transform, Continuous wavelet transform, Discrete wavelet transform, wavelet series, Interpretations of the Time-Frequency plot.

UNIT II

**Transforms:** Walsh, Hadamard, Haar and Slant Transforms, DCT, DST, KLT, Singular value Decomposition – definition, properties and applications

UNIT III

**Continuous Wavelet Transform (CWT):** Shortcomings of STFT, Need for wavelets, Wavelet Basis- Concept of Scale and its relation with frequency, Continuous time wavelet Transform Equation- Series Expansion using Wavelets- CWT- Tiling of time scale plane for CWT. Important Wavelets: Haar, Mexican Hat, Meyer, Shannon, Daubechies.

UNIT IV

**Multi Rate Analysis and DWT:** Need for Scaling function – Multi Resolution Analysis, Two-Channel Filter Banks, Perfect Reconstruction Condition, Relationship between Filter Banks and Wavelet Basis, DWT, Structure of DWT Filter Banks, Daubechies Wavelet Function, Applications of DWT.

UNIT V

**Wavelet Packets and Lifting:** Wavelet Packet Transform, Wavelet packet algorithms, Thresholding-Hard thresholding, Soft thresholding,
Multidimensional Wavelets, Bi-orthogonal basis- B-Splines, Lifting Scheme of Wavelet Generation, Multi Wavelets

TEXTBOOKS:

REFERENCE BOOKS:
UNIT-I

**VLSI Technology**: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

**VLSI Design**: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II

**CMOS VLSI Design**: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes.

**Building Blocks of a VLSI circuit**: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces.

**VLSI Design Issues**: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-III

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitative and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-IV

**Subsystem Design and Layout**: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

**Subsystem Design Processes**: Some general considerations and an illustration of design processes, design of an ALU subsystem.
UNIT-V

Floor Planning: Introduction, Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS:

REFERENCE BOOKS:
UNIT-I

**Signal models and characterization**: Types and properties of statistical models for signals and how they relate to signal processing. Common second-order methods of characterizing signals including autocorrelation, partial correlation, cross-correlation, power spectral density and cross-power spectral density.

UNIT-II

**Spectral estimation**: Nonparametric methods for estimation of power spectral density, autocorrelation, cross-correlation, transfer functions, and coherence from finite signal samples.

UNIT-III

**Review of signal processing**: A review on random processes, a review on filtering random processes, Examples.

**Statistical parameter estimation**: Maximum likelihood estimation, maximum a posteriori estimation, Cramer-Rao bound.

UNIT-IV

**Eigen structure based frequency estimation**: Pisarenko, MUSIC, ESPRIT, their application in sensor array direction finding.

**Spectrum estimation**: Moving average (MA), Auto Regressive (AR), Auto Regressive Moving Average (ARMA), Various non-parametric approaches.

UNIT-V

**Wiener filtering**: The finite impulse case, causal and non-causal infinite impulse responses cases, Least mean squares adaptation, recursive least squares adaptation, Kalman filtering.

**TEXTBOOKS:**


**REFERENCE BOOKS:**

UNIT –I

**Signal propagation in Optical Fibers**: Geometrical Optics approach and Wave Theory approach, Loss and Bandwidth, Chromatic Dispersion, Non Linear effects- Stimulated Brillouin and Stimulated Raman Scattering, Propagation in a Non-Linear Medium, Self-Phase Modulation and Cross Phase Modulation, Four Wave Mixing, Principle of Solitons.

UNIT –II

**Fiber Optic Components for Communication & Networking**: Couplers, Isolators and Circulators, Multiplexers, Bragg Gratings, Fabry-Perot Filters, Mach Zender Interferometers, Arrayed Waveguide Grating, Tunable Filters, High Channel Count Multiplexer Architectures, Optical Amplifiers, Direct and External Modulation Transmitters, Pump Sources for Amplifiers, Optical Switches and Wavelength Converters.

UNIT –III


UNIT –IV

**Transmission System Engineering**: System Model, Power Penalty in Transmitter and Receiver, Optical Amplifiers, Crosstalk and Reduction of Crosstalk, Cascaded Filters, Dispersion Limitations and Compensation Techniques.

UNIT –V

**Fiber Non-linearities and System Design Considerations**: Limitation in High Speed and WDM Systems due to Non-linearities in Fibers,
Wavelength Stabilization against Temperature Variations, Overall System Design considerations – Fiber Dispersion, Modulation, Non-Linear Effects, Wavelengths, All Optical Networks.

TEXT BOOKS:

REFERENCE BOOKS:
PART-A: VLSI Lab (Front-end Environment)

- The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/ Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/ FPGA kits).

- The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least FOUR experiments on each Platform.

List of Experiments:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter.
4. Synchronous RAM.
5. ALU.
6. UART Model.
7. Traffic Light Controller using Sequential Logic circuits
8. Finite State Machine (FSM) based logic circuit.

PART-B: VLSI Lab (Back-end Environment)

- The students are required to design and implement the Layout of the following experiments of any THREE using CMOS 130nm Technology with Mentor Graphics Tool.
List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Digital-to-Analog-Converter.

LAB REQUIREMENTS FOR PART-A AND PART-B:


**Hardware:** Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

PART-C: Embedded Systems Laboratory

- The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits.

- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.

- The students are required to perform at least THREE experiments.

List of Experiments: (using ARM-926 with PERFECT RTOS)

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.

6. Avoid deadlock using BANKER’S algorithm.

**Lab Requirements for PART-C:**

**Software:**

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library

(ii) LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

**Hardware:**

(i) The development kits of ARM-926 Developer Kits Boards.

(ii) Serial Cables, Network Cables and recommended power supply for the board.
UNIT –I

**Coding for Reliable Digital Transmission and Storage:** Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

**Linear Block Codes:** Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT –II

**Cyclic Codes:** Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT –III

**Convolutional Codes:** Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT –IV

**Burst –Error-Correcting Codes:** Decoding of Single-Burst error Correcting Cyclic codes, Single-Burst-Error-Correcting Cyclic codes, Burst-Error-Correcting Convolutional Codes, Bounds on Burst Error-Correcting Capability, Interleaved Cyclic and Convolutional Codes, Phased-Burst –Error-Correcting Cyclic and Convolutional codes.
UNIT-V

**BCH – Codes:** BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes- Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction

**TEXTBOOKS:**


**REFERENCE BOOKS:**

1. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
3. Introduction to Error Control Codes-Salvatore Gravano-oxford
5. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Ed, 2009, TMH.
UNIT-I


UNIT-II

RTOS Programming Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-III

Program Modeling – Case Studies Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-IV


Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming.
Programming in RT Linux Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.

TEXT BOOKS:


REFERENCES:


## I – II

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### IMAGE AND VIDEO PROCESSING

## UNIT–I

**Fundamentals of Image Processing and Image Transforms:**

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform

Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

## UNIT–II

**Image Enhancement:** Spatial domain methods: Histogram processing. Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

**Frequency domain methods:** Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

**Image Restoration:** Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

## UNIT–III

**Image Segmentation:** Introduction to image segmentation, Point, Line and Edge Detection, Region based segmentation., Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

**Image Compression:** Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image

UNIT-IV

**Basic Steps of Video Processing:** Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT-V

**2-D Motion Estimation:** Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXTBOOKS:

REFRENCE BOOKS:
UNIT I


UNIT II


UNIT III

Mobile Radio Propagation: Small Scale Fading and Multipath: Small Scale Multipath propagation - Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel - Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements - Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels.
Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke’s model for flat fading, spectral shape due to Doppler spread in Clarke’s model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT-IV


UNIT-V

**Wireless Networks** Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

**TEXTBOOKS:**

REFERENCE BOOKS:

2. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
UNIT-I


**MOS Design** Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

**Combinational MOS Logic Circuits**: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

**Sequential MOS Logic Circuits** Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-III

**Dynamic Logic Circuits** Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

**Semiconductor Memories** Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.
UNIT-IV

**Analog CMOS Sub-Circuits** MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT-V

**CMOS Amplifiers** Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.


TEXTBOOKS:


REFERENCE BOOKS:

3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
UNIT -I

**Fundamentals of Computer Design:** Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, Measuring and reporting performance, Quantitative principles of computer design, Amdahl’s law.

Instruction set principles and examples- Introduction, Classifying instruction set- MEmory addressing- type and size of operands, Operations in the instruction set.

UNIT –II

**Pipelines:** Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

**Memory Hierarchy Design:** Introduction, Review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT-III

**Instruction Level Parallelism the Hardware Approach:** Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, high performance instruction delivery- hardware based speculation.

**ILP Software Approach** Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT-IV

**Multi Processors and Thread Level Parallelism:** Multi Processors and Thread level Parallelism- Introduction, Characteristics of
application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT –V

**Inter Connection and Networks:** Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of interconnection, Cluster, Designing of clusters.

**Intel Architecture:** Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

**TEXTBOOKS:**

**REFERENCE BOOKS:**
UNIT – I

**Introduction to Digital Signal Processing:** Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

**Computational Accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT – II

**Architectures for Programmable DSP Devices:** Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT – III

**Programmable Digital Signal Processors:** Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX Processors.

UNIT – IV

**Analog Devices Family of DSP Devices:** Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base
Architecture of ADSP 2100, ADSP-2181 high performance Processor. 
Introduction to Blackfin Processor - The Blackfin Processor, 
Introduction to Micro Signal Architecture, Overview of Hardware 
Processing Units and Register files, Address Arithmetic Unit, Control 
Unit, Bus Architecture and Memory, Basic Peripherals. 

UNIT –V

Interfacing Memory and I/O Peripherals to Programmable DSP 
Devices: Memory space organization, External bus interfacing signals, 
Memory interface, Parallel I/O interface, Programmed I/O, Interrupts 
and I/O, Direct memory access (DMA).

TEXT BOOKS:
1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson 
2. A Practical Approach to Digital Signal Processing - K Padmanabhan, 
3. Embedded Signal Processing with the Micro Signal Architecture 

REFERENCE BOOKS:
1. Digital Signal Processors, Architecture, Programming and Applications 
   – B. Venkataramani and M. Bhaskar, 2002, TMH.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et 
   al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family 
   by The Applications Engineering Staff of Analog Devices, DSP Division, 
   Edited by Amy Mar, PHI
5. The Scientist and Engineer’s Guide to Digital Signal Processing by 
   Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0- 
   9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of 
   Analog Devices, Newnes, ISBN 0750679123, 2005
UNIT-I

Introduction, Natural and Nuclear Sources of EMI / EMC:
Electromagnetic environment, History, Concepts, Practical experiences and concerns, frequency spectrum conservations, An overview of EMI / EMC, Natural and Nuclear sources of EMI.

UNIT-II

EMI from Apparatus, Circuits and Open Area Test Sites:
Electromagnetic emissions, Noise from relays and switches, Non-linearities in circuits, passive intermodulation, Cross talk in transmission lines, Transients in power supply lines, Electromagnetic interference (EMI), Open area test sites and measurements.

UNIT-III:

Radiated and Conducted Interference Measurements and ESD:
Anechoic chamber, TEM cell, GH TEM Cell, Characterization of conduction currents / voltages, Conducted EM noise on power lines, Conducted EMI from equipment, Immunity to conducted EMI detectors and measurements, ESD, Electrical fast transients / bursts, Electrical surges.

UNIT-IV:

Grounding, Shielding, Bonding and EMI filters: Principles and types of grounding, Shielding and bonding, Characterization of filters, Power lines filter design.

UNIT-V:

Cables, Connectors, Components and EMC Standards: EMI suppression cables, EMC connectors, EMC gaskets, Isolation transformers, optoisolators, National / International EMC standards.
TEXT BOOKS:


REFERENCE BOOKS:

ADVANCED COMMUNICATIONS LAB

Note:

1. Minimum of 10 Experiments have to be conducted
2. All Experiments may be Simulated using MATLAB and to be verified using related training kits.
   1. Measurement of Bit Error Rate using Binary Data
   2. Verification of minimum distance in Hamming code
   3. Determination of output of Convolutional Encoder for a given sequence
   4. Determination of output of Convolutional Decoder for a given sequence
   5. Efficiency of DS Spread- Spectrum Technique
   6. Simulation of Frequency Hopping (FH) system
   7. Effect of Sampling and Quantization of Digital Image
   8. Verification of Various Transforms (FT / DCT/ Walsh / Hadamard) on a given Image (Finding Transform and Inverse Transform)
   9. Point, Line and Edge detection techniques using derivative operators.
   10. Implementation of FIR filter using DSP Trainer Kit (C-Code/ Assembly code)
   11. Implementation of IIR filter using DSP Trainer Kit (C-Code/ Assembly code)
   12. Determination of Losses in Optical Fiber
   13. Observing the Waveforms at various test points of a mobile phone using Mobile Phone Trainer
   15. Study of ISDN Training System with Protocol Analyzer